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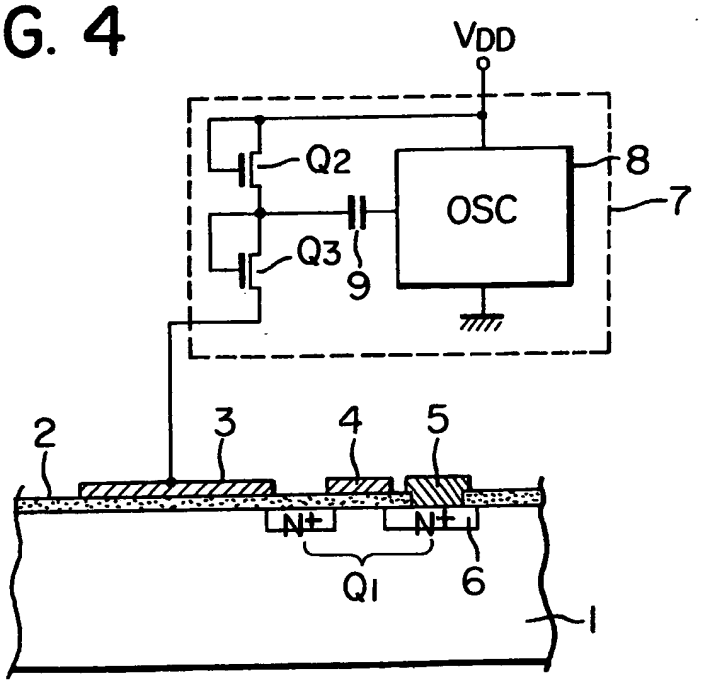
(54) **Semiconductor memory device**

(57) A semiconductor memory is provided with an on-chip circuit 7 for supplying a stepped-up voltage to the plate 3 of an MIS storage capacitor. The memory comprises an array of one-transistor one-capacitor dynamic RAM cells and the provision of a higher capacitor plate voltage permits a reduction in capacitor area, and hence an increase in packing density, while maintaining sufficient charge storage capacity.

The voltage generator comprises a pair of transistors Q2, Q3 and a capacitor arranged as a voltage pump driven by an oscillator 8 which may comprise a plurality of inverters connected via a ring. A further transistor (Q4) may be connected across transistors Q2 and Q3 (ie between V_{DD} and capacitor plate 3) to limit the output voltage at a level equal to its threshold voltage above V_{DD}.

FIG. 4



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The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

ments thereof taken in conjunction with the accompanying drawings.

Brief description of the drawings

Figure 1 is a sectional view of a prior art single transistor storage cell;

Figure 2 is a view similar to Figure 1 which is used for the explanation of the write operation when a bit line is maintained at a low level;

Figure 3 is a view also similar to Figure 1 which is used for the explanation of the write operation when the bit line is maintained at a high level;

Figure 4 is a schematic sectional view of a first embodiment of the present invention;

Figure 5 is a detailed diagram of an oscillator circuit shown in Figure 4;

Figure 6 is a schematic sectional view of the oscillator circuit shown in Figure 5 when it is formed on a chip of semiconductor;

Figure 7 is a schematic sectional view of two transistors Q_2 and Q_3 and a capacitor of the oscillator circuit shown in Figure 5 when they are formed on the same chip shown in Figure 6;

Figure 8 shows an output voltage characteristic of the cell plate voltage generating circuit of the first embodiment;

Figure 9 is a schematic sectional view of a second embodiment of the present invention;

Figure 10 is a schematic sectional view of a cell plate voltage generating circuit of the second embodiment when it is formed on a chip of semiconductor;

Figure 11 shows an output voltage characteristic of the cell plate voltage generating circuit of the second embodiment;

Figure 12 shows the relationship between the power supply voltage V_{DD} and the voltage swing across a MIS capacitor in the single transistor storage cell; and

Figure 13 shows the relationship between the power supply voltage V_{DD} and the voltage of the signal derived with a differential sense amplifier which directly detects the electric charge stored on a MIS capacitor.

Same reference numerals are used to designate similar parts throughout the figures.

Description of the preferred embodiments

Prior art, Figures 1 through 3

First referring to Figures 1 through 3, a prior art single transistor cell, the improvement of which is the object of the present invention, will be described. Figure 1 shows the construction of a memory cell of an N-channel MIS FET. Over a P-type silicon substrate 1 is grown a silicon oxide film 2 on which is deposited or otherwise formed a memory cell plate 3 which is a film of a metal such as molybdenum and which functions as an electrode. Thus a charge storage MIS capacitor is provided. A MIS FET Q_1 is formed with N^+ diffusion layers 6 connected to a word line 4 and a bit line 5 and the MIS capacitor.

When a DC voltage is supplied to the memory plate 3, a "potential well" is formed in the MIS capacitor. In order to write information, the bit line 5 is raised to a high level or is lowered to a low level and the word line 4 is activated to a high potential so that the transistor Q_1 is turned on and electric charge is inplanted from the bit line 5 to the MIS capacitor, whereby the information "1" or "0" is stored. The information "0" or "1" is stored by drawing the electric charge from the MIS capacitor to the bit line 5.

Figure 2 shows the storage of information into the memory cell when the bit line 5 is maintained at a low level. The "potential well" below the diffusion layer 6 connected to the bit line 5 is shallow as compared with the "potential well" below the MIS capacitor so that the electric charge flows from the bit line 5 into the MIS capacitor and is stored on it. Thus the information is stored in the memory cell. The lower the bit line 5, the more electric charge can migrate into the memory cell. It follows, therefore, that the bit line 5 is in general grounded.

Figure 3 shows the storage of information when the bit line 5 is maintained at a high level. The depth of the "potential well" below the diffusion layer 6 connected to the bit line 5 is made equal to or the same as the depth of the "potential well" below the MIS capacitor so that all the electric charge stored on the MIS capacitor migrates into the bit line 5.

Of a voltage applied to the memory cell plate 3, an effective amplitude voltage which serves to form a "potential well" is the difference between the voltage applied to the memory cell plate 3 and a MIS threshold voltage V_{TH} of the MIS capacitor. The voltage applied to the memory cell plate 3 will not exceed a V_{DD}, a supply voltage applied to the chip for the particular technology, and is equal to V_{DD} at the maximum. As a result, the depth of the "potential well" below MIS capacitor is dependent upon a MIS capacitor voltage expressed by

$$V_{DD} - V_{TH}$$

and the maximum quantity of the stored charge is dependent upon the depth of the "potential well" created. In writing information, when the depth of the "potential well" below the diffusion layer 6 is equal in depth to the "potential well" created by $V_{DD} - V_{TH}$, then the "potential well" below the MIS capacitor can be emptied. It follows, therefore, that it suffices to raise the potential of the bit line 5 to a level higher than $V_{DD} - V_{TH}$.

As described above, according to the prior art, even when the potential of the bit line 5 is swung fully from GND to V_{DD}, the stored charge is limited by $V_{DD} - V_{TH}$.

The present invention relates to a single transistor cell of the type described above and is characterized by the provision of a cell plate voltage generating circuit capable of generating a DC voltage higher than V_{DD} on a chip on which are arranged memory cells.

First embodiment, Figures 4 through 8

Figure 4 shows the construction of a first embodiment of the present invention. An output terminal of a cell plate voltage generating circuit 7 is connected

to the memory cell plate 3 of the memory cell. The cell plate voltage generating circuit 7 comprises an oscillator circuit 8, a capacitor 9 and two transistors Q_2 and Q_3 which are connected in series. An input terminal of the oscillator circuit 8 is connected to a power supply V_{DD} and an output terminal thereof is connected through the capacitor 9 to the junction between the series-connected transistors Q_2 and Q_3. The gate of the upper transistor Q_2 is connected to the power supply V_{DD} and the gate of the lower transistor Q_3 is connected to the junction between Q_2 and Q_3. One end of the series-connected circuit is connected to the power supply and the other end, to the output terminal of the cell plate voltage generating circuit.

Figure 5 is a detailed diagram of the oscillator circuit 8 which is a ring oscillator consisting of a number of n (where n is an odd integer) stages of inverters each consisting of series-connected transistors Q_{i1} and Q_{i2}. The junction between the transistors Q_{i1} and Q_{i2} in the preceding inverter is connected to the gate of the lower transistor $Q_{(i+1)2}$ of the succeeding inverter, and the junction between the transistors in the last stage inverter is connected to the gate of the lower transistor Q_{i2} of the first stage inverter. The upper ends of the inverters are connected to the power supply V_{DD} and the lower ends are grounded.

Figure 6 shows the cross section of one inverter of the oscillator circuit 8 which is formed on the same chip upon which are formed memory cells. Reference numeral 1 denotes a P-type silicon substrate; 10, 11 and 12 are N^+ diffusion layers or islands formed in the substrate or wafer 1 and serve as the source or drain regions of the transistors Q_{i1} and Q_{i2}; 13, a silicon oxide film; 14, a gate oxide film; 15 and 16, polysilicon (POLY) gate electrodes of the transistors Q_{i1} and Q_{i2}, respectively; 17 through 20, terminals of aluminium or the like.

The terminal 17 is the upper end of the inverter and is connected to the source region 10 and the gate electrode 15 of the transistor Q_{i1} is connected to the power supply V_{DD}. The terminal 18 which is the lower end of the inverter pair and is connected to the drain region 12 of the transistor Q_{i2} is grounded. The terminal 19 which is connected to the gate electrode of the transistor Q_{i2} is connected to the preceding inverter pair, and the terminal 20 which is connected to the region 11 which is the junction between the transistors Q_{i1} and Q_{i2} is connected to the succeeding inverter pair.

Figure 7 shows in detail the cross section of the transistors Q_2 and Q_3 and the capacitor 9 of the cell plate voltage generating circuit 7. Reference numeral 1 denotes a P-type silicon wafer; 21 through 24, N^+ diffusion layers or islands in the wafer 1 and the source or drain regions of the transistors Q_2 and Q_3; 13, a silicon oxide film; 14, a gate oxide film; 25 and 26, polysilicon gates of Q_2 and Q_3, respectively; 27, polysilicon, one of the end of the capacitor 9; and 28 through 32, terminals of aluminium or the like.

The terminal 28 which is connected to the source region and the gate electrode of the transistor Q_2 is connected to the power supply V_{DD}. The terminal 29 which is connected to the drain region 22 of the transistor Q_2 is connected via the terminal 30 to the source region 23 and the gate electrode 26 of the transistor Q_3 and is one end of the capacitor 9. The terminal 31 which is connected to the other electrode 27 of the capacitor 9 is connected to the output terminal of the oscillator circuit 8. The output terminal 32 which is connected to the drain region 24 of the transistor Q_3 is connected to the cell plate 3.

As is apparent from Figures 6 and 7, the cell plate voltage generating circuit 7 can be formed with MIS FETs and MIS capacitors with which the single transistor cell is formed. In other words, the cell plate voltage generating circuit 7 can be fabricted with the same materials as the single transistor cell. Thus the integrated cell plate voltage generating circuit and memory cell can be formed on the same chip.

Next the mode of operation of the cell plate voltage generating circuit 7 will be described with reference to Figure 3. In response to the output signal from the oscillator circuit 8, the transistors Q_2 and Q_3 are alternately turned on and off so that the electric charge is pumped from the power supply V_{DD} to the output terminal. As a result, a DC voltage is created at the output terminal, the magnitude of this DC voltage being depending upon the circuit parameters such as the amplitude of the output signal of the oscillator circuit 8. The DC output voltage becomes higher than the power supply voltage V_{DD}.

The relationship between the output voltage V of the cell plate voltage generating circuit 7 and the power supply voltage V_{DD} is shown in Figure 8. The power supply voltage V_{DD} is plotted along the abscissa and the output voltage from the cell plate voltage generating circuit 7 is plotted along the ordinate. The characteristic curve (a) indicates the voltage applied to the cell plate 3 when no cell plate voltage generating circuit is used. In this case, as described previously, the maximum voltage applied to the cell plate 3 is equal to the power supply voltage V_{DD}. When the cell plate voltage generating circuit in accordance with the present invention is integrated, the voltage higher than the power supply V_{DD} can be applied to the cell plate 3 as indicated by the characteristic curve (b).

When the high DC output voltage from the cell plate voltage generating circuit 7 is applied to the memory cell plate 3, the depth of the "potential well" created below the MIS capacitor can be increased by a degree corresponding to the difference between the output voltage from the cell plate voltage generating circuit 7 and the power supply voltage V_{DD}. As a result, the electric charge stored on the MIS capacitor can be increased accordingly. In addition, the potential on the bit line 5 can be swung more widely in controlling the electric charge stored in the memory cell. When the output voltage from the cell plate voltage generating circuit 7 exceeds the sum of V_{DD} and V_{TH}, the swing of the potential on the bit line from GND to V_{DD} can contribute very effectively on the control of the electric charge stored in the memory cell. As a consequence, the difference in terms of the stored electric charge between the information "0" and "1" can be made more distinguished from each other so that the stable storage

operation can be ensured.

It suffices to apply a voltage at a predetermined level to the memory cell plate 3 and it is not needed at all to supply a current to the plate so that the power consumption can be reduced. For instance, with a power supply voltage of 5 V, the power consumption is of the order of 5 mW.

Second embodiment, Figures 9 through 13

A second embodiment shown in Figure 9 is substantially similar in construction to the first embodiment shown in Figure 4 except that a transistor Q_4 is added which functions as a voltage limitter circuit so as to prevent the output voltage from the cell plate voltage generating circuit 7 from rising above $V_{DD} + V_{TH}$. It only suffices to swing the potential on the bit line 5 between GND and V_{DD}. In other words, it is not needed to apply a voltage higher than $V_{DD} + V_{TH}$ to the memory cell plate 3. The application of a higher voltage results in breakdowns of the chip.

While the voltage; that is, the output voltage from the memory cell voltage generating circuit 7 and the stability of this voltage are dependent upon the performance of the circuit 7 itself in the first embodiment, the second embodiment is featured in that the output voltage from the cell plate voltage generating circuit 7 is set to a level slightly higher than $V_{DD} + V_{TH}$ so that the voltage actually applied to the memory cell plate 3 can be stabilized at $V_{DD} + V_{TH}$.

Figure 10 shows the cross section of the cell plate voltage generating circuit of the second embodiment which is substantially similar in construction to the first embodiment shown in Figure 7 except the addition of the transistor Q_4. The transistor Q_4 comprises the gate oxide film 14, the source region 33 and drain region 34 consisting of N^+ diffusion layers or islands, a polysilicon gate electrode 35 and conducting terminal or electrodes 36 and 37 of aluminium or the like. The terminal or electrode 36 connected to the source region 33 of the transistor Q_4 is connected to the source region and the gate electrode of the transistor Q_2 and to the power supply source V_{DD}. The terminal or electrode 37 which is connected to the drain region and the gate electrode 35 of the transistor Q_4 is connected via the terminal or electrode 32 to the drain region of the transistor Q_3 and to the cell plate 3. Since the transistor Q_4 is MOS FET, it can be formed on the same chip.

Figure 11 shows the characteristic curve (c) of the cell plate voltage generating circuit of the second embodiment. The curves (a) and (b), which have been explained already with reference to Figure 8 are added for the sake of comparison. It is readily seen that as compared with the characteristic curve (b) of the first embodiment, the curve (c) is closer to and parallel with the (a). This means that the output voltage from the circuit 7 is controlled at V_{DD} and V_{TH} and applied to the memory cell plate 3.

Next referring to Figure 12, the mode of operation of the second embodiment of the present invention will be described in detail in comparison with a prior art memory cell. Figure 12 shows the relationship between the power supply voltage V_{DD} supplied from a single power supply to a semiconductor memory device and the amplitude of the voltage in a cell. In the following discussion, the power supply voltage is assumed to be 5 V. The prior art memory cell has a leakage loss of about 0.7 V, a loss of about one V corresponding to one α ray, a threshold voltage loss of about 1 V due to the MIS construction and a noise loss of about 0.6 V. As a result, the amplitude of the voltage in the cell is about 1.7 V. When the power supply voltage is decreased, the amplitude of the voltage within the cell becomes zero when V_{DD} is about 2.5 V so that no output signal can be derived from the prior art cell. This means that with the prior art cell, the lowering of the power supply voltage is limited.

According to the second embodiment of the present invention, the cell plate voltage generating circuit 7 steps up the power supply voltage of 5 V by one volt, which corresponds to the V_{TH} loss, to 6 V which in turn is applied the memory cell plate 3. Thus the threshold loss is compensated for. As a result the amplitude of the voltage in the cell becomes about 2.6 V, which is about 160% as high as that of the prior art memory cell. Subsequently, at the power supply voltage of about 2.5 V at which the prior art memory cell cannot operate as described previously, the amplitude of about 1 V can be obtained. This means that the present invention can lower the power supply voltage. It is obvious that when the cell plate voltage generating circuit 7 steps up the power supply voltage by a voltage higher than V_{TH}, the voltage amplitude can be further increased so that the power supply voltage can be lowered. The ratio of α ray loss against the amplitude of the voltage in the cell can be lowered because of the compensation for the threshold voltage loss.

When the electric charge stored on the MIS capacitor with the voltage swing in the cell described above is detected by a differential sense amplifier, the sensed signal voltage becomes 1/10 of the voltage amplitude in the cell which is dependent upon the ratio in capacitance between the bit line and the MIS capacitor. The relationship between the signal voltage Vsig and the power supply voltage V_{DD} is shown in Figure 13. Since the power supply voltage of 5 V fluctuates by $\pm$ 10%, the present invention is compared with the prior art at the power supply voltage of 4.5 V. 4.5 V is the widest fluctuation from the power supply voltage V_{DD} of 5 V when the fluctuation in reference voltage and threshold voltage of the transistor are taken into consideration when the fluctuation of the power supply voltage is about 10%. Then the signal voltage amplitude of the prior art is about 56 mV, but that of the present invention is about 97 mV which is about 70% higher than the former. The prior art cannot detect the signal voltage when the power supply voltage is less than 3 V because of the fluctuation in threshold voltage of the transistor, but the present invention can detect the signal voltage of about 50 mV even at the same power supply voltage of 3.5 V.

According to the present invention, a higher signal voltage can be detected as compared with the prior

FIG. 11

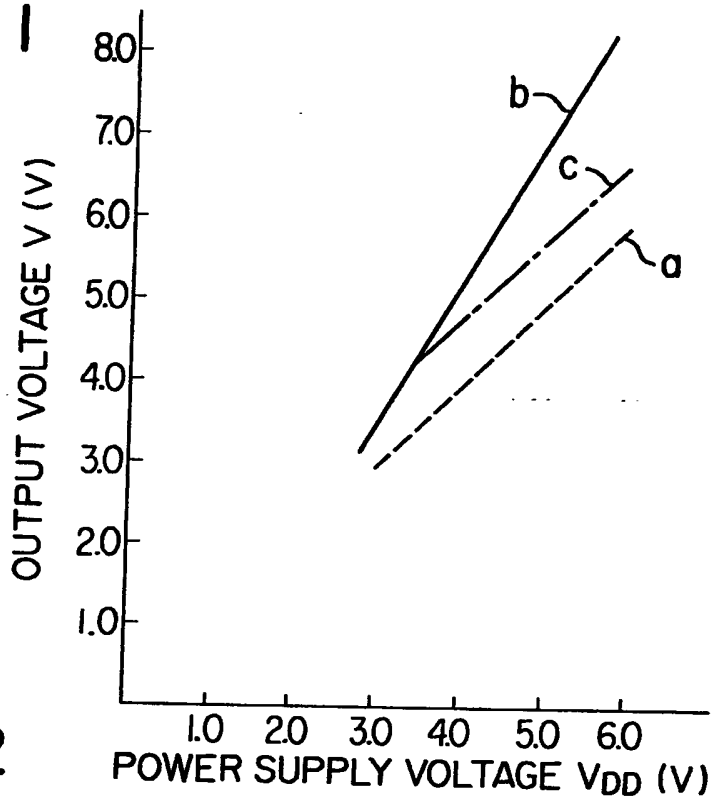
OUTPUT VOLTAGE V (V)
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
b
c
a
1.0 2.0 3.0 4.0 5.0 6.0
POWER SUPPLY VOLTAGE VDD (V)

FIG. 12

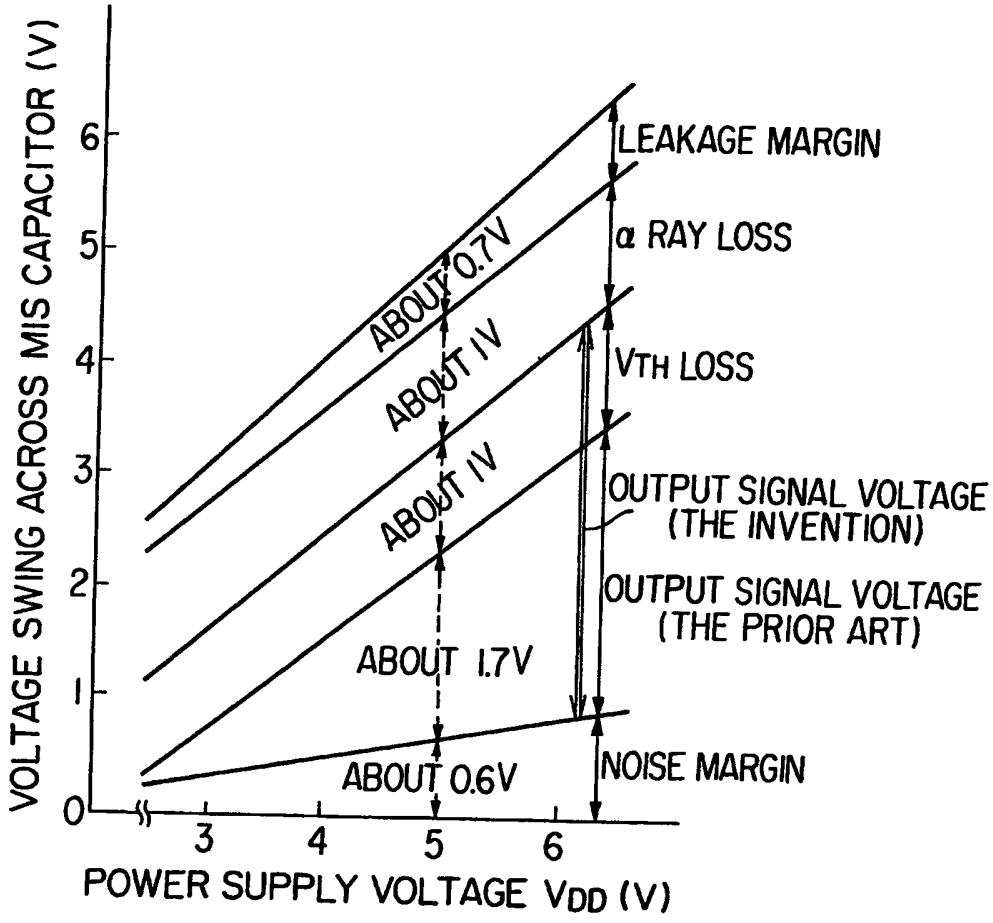
VOLTAGE SWING ACROSS MIS CAPACITOR (V)
0
1
2
3
4
5
6
LEAKAGE MARGIN
α RAY LOSS
VTH LOSS
OUTPUT SIGNAL VOLTAGE (THE INVENTION)
OUTPUT SIGNAL VOLTAGE (THE PRIOR ART)
NOISE MARGIN
ABOUT 0.7V
ABOUT 1V
ABOUT 1V
ABOUT 1.7V
ABOUT 0.6V
3 4 5 6
POWER SUPPLY VOLTAGE VDD (V)

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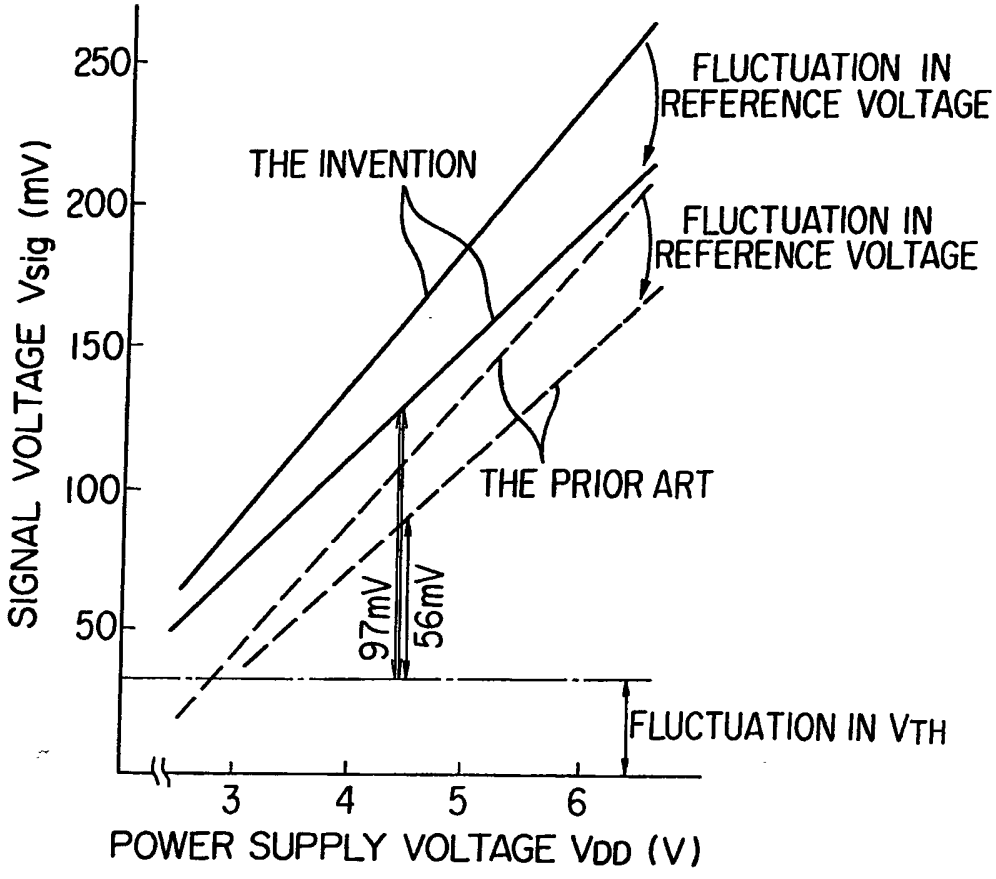
FIG. 13



SPECIFICATION

Semiconductor memory device

Background of the invention

The present invention relates to a semiconductor memory device.

Various types of semiconductor memory devices have been devised and improved in order to attain higher density, higher speed and higher reliability. In the MOS random access memory (MOS RAM), one memory cell consists of a single transistor storage cell consisting of one MIS FET (Metal-Insulated Semiconductor Field-Effect Transistor) and one MIS capacitor. Such single transistor cell semiconductor memory device is disclosed in detail in, for instance, IEEE Journal of Solid-State Circuits, Vol. SC-7, No. 5, Oct. 1972. The single transistor cell semiconductor memory devices now dominate the MOS RAM market because a minimum number of parts are used and subsequently a higher degree of packaging density can be attained.

In the conventional single transistor cell of the type described above, a voltage applied to a memory cell plate will not exceed a power supply voltage V_{DD} applied to a chip of semiconductor and is equal to V_{DD} at the maximum. As a result, the depth of a "potential well" created by a MIS capacitor is dependent upon a voltage swing across the MIS capacitor; tthat is the difference between V_{DD} and a MIS threshold voltage V_{TH}, i.e., $V_{DD} - V_{TH}$. The maximum electric charge storable on the MIS capacitor is then dependent upon the depth of the "potential well" created.

The read operation of the single transistor cell is accomplished by directly sensing the electric charge stored on the MIS capacitor. It follows, therefore, that the higher the electric charge stored on the MIS capacitor, the more stable the read and write operations become. The maximum value of the electric charge stored on a MIS capacitor is dependent upon the capacitance of this capacitor and a swing or change in amplitude of a voltage applied thereacross.

In order to attain a higher packaging density of MOS RAM, the surface area of each memory cell must be reduced and consequently the area occupied by each MIS capacitor must be decreased. An unavoidable result is then the reduction in capacitance of MIS capacitors. In addition, in order to avoid the electrical breakdowns of insulating films, the power supply voltage must be lowered. However, the lowering of the threshold voltage V_{TH} of the MIS capacitor in proportion to the lowering of the power supply voltage V_{DD} is difficult because of the fluctuation in performance and characteristics of circuits. As a result, as the power supply voltage V_{DD} of MOS RAM is lowered with increase in packaging density, the ratio of the threshold loss in the swing or change in amplitude of a voltage applied across a MIS capacitor suddenly rises with the resultant decrease of a voltage swing across the capacitor.

Thus the attempts for increasing the packaging density of single transistor storage cell memory devices result in the decrease not only in the capacitance of MIS capacitors but also in the voltage swing across them, of which decrease in turn results in the reduction in electric charge stored on the MIS capacitor. However, for the stable and reliable read operation, sufficient electric charge must be stored. Thus there has been a limit to the increasing the packaging density of MOS RAM. In addition, when the stored electric charge is reduced, the soft error due to the α ray generated from packaging media will adversely affect the signal voltage. As a result, it becomes further difficult to provide the highly reliable semiconductor memory devices. Furthermore, in order to read out a small quantity of stored electric charge, a sense amplifier with a higher degree of sensitivity is needed, but the increase in sensitivity is again limited by the circuit arrangements.

In summary, it has been extremely difficult to provide a single transistor storage cell type semiconductor memory device which has a higher degree of packaging density and a higher degree of reliability.

Summary of the invention

In view of the above, one of the objects of the present invention is to provide an improved semiconductor memory device which has a higher degree of packaging density and is highly reliable and dependable in operation.

Another object of the present invention is to provide an improved semiconductor device which can operate in a satisfactorily stable manner even at a low power supply voltage.

A further object of the present invention is to provide an improved semiconductor memory device in which voltage step-up circuits, which are highly compatible with single transistor storage cells in the fabrication process, are formed on the same chip of the storage cells so that the electric charge stored on each MIS capacitor can be increased, the resistance to soft errors can be improved and highly reliable operations can be ensured.

A yet another object of the present invention is to provide an improved semiconductor memory device which needs not a high-sensitivity sense amplifier for the read operation.

To the above and other ends, briefly stated, the present invention provides a semiconductor memory device of the type in which a storage cell is a MIS capacitor defined by a semiconductor substrate, an insulating film formed over the semiconductor substrate and a memory cell plate which is formed over the insulating film and is an electrode, said semiconductor memory device being characterized by the provision of a cell plate voltage generating circuit which is also formed on the semiconductor substrate and adapted to supply a DC voltage higher than a power supply voltage V_{DD} supplied to the semiconductor memory device.

The present invention is further characterized in the provision of a voltage limitter circuit for limiting the output voltage from the cell plate voltage generating circuit.

The above and other objects, effects and features of the present invention will become more apparent from the following description of preferred embodi-

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FIG. 1

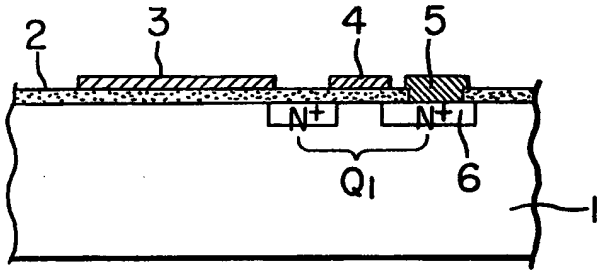

FIG. 2

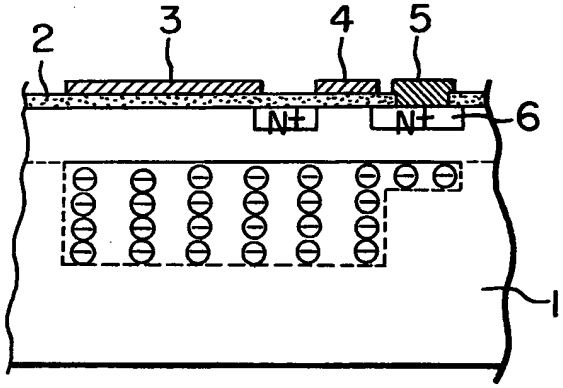

FIG. 3

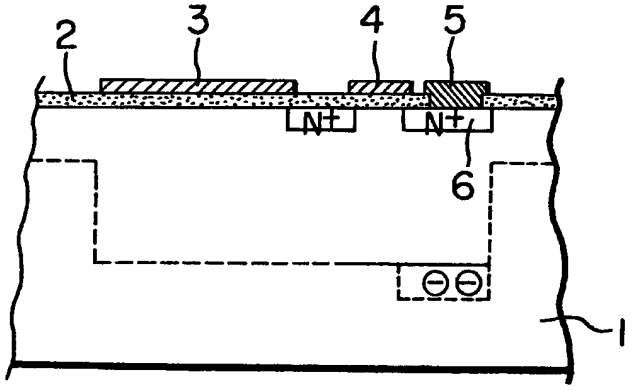

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FIG. 4

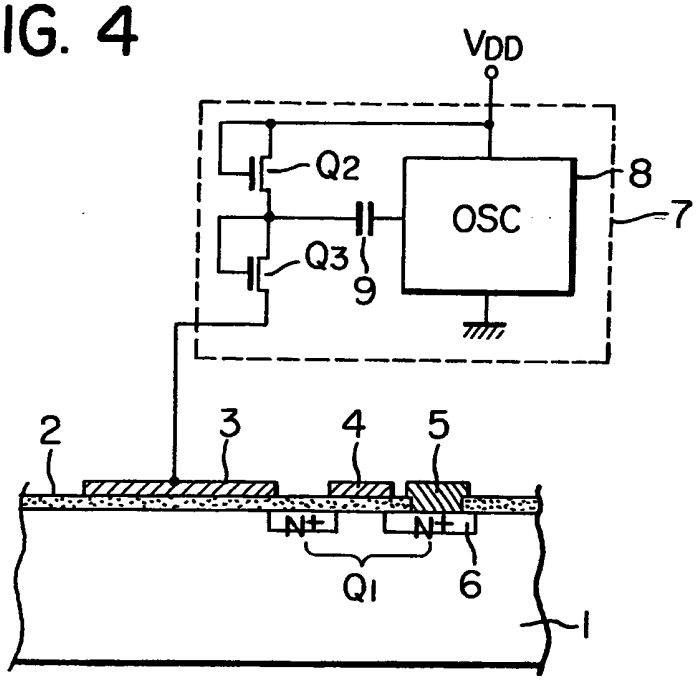
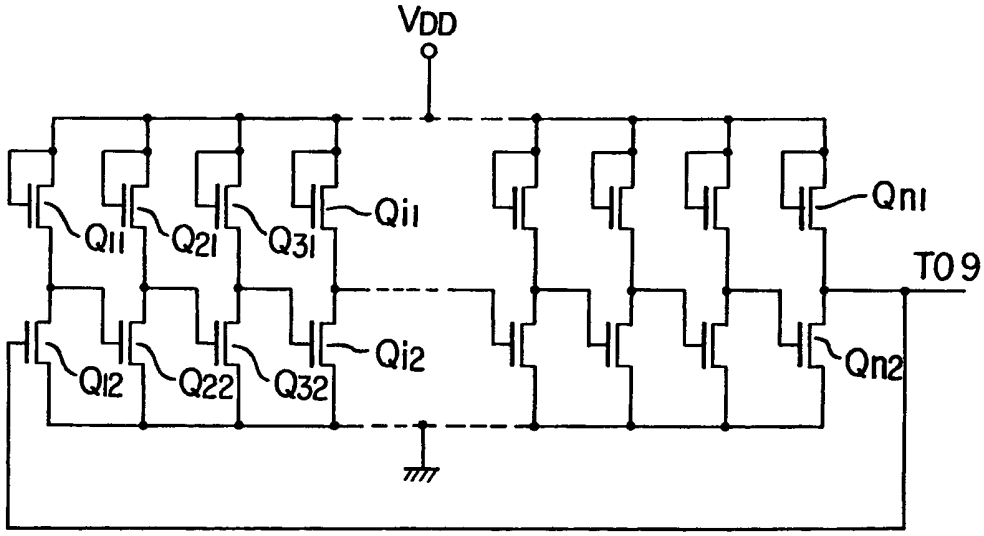


FIG. 5



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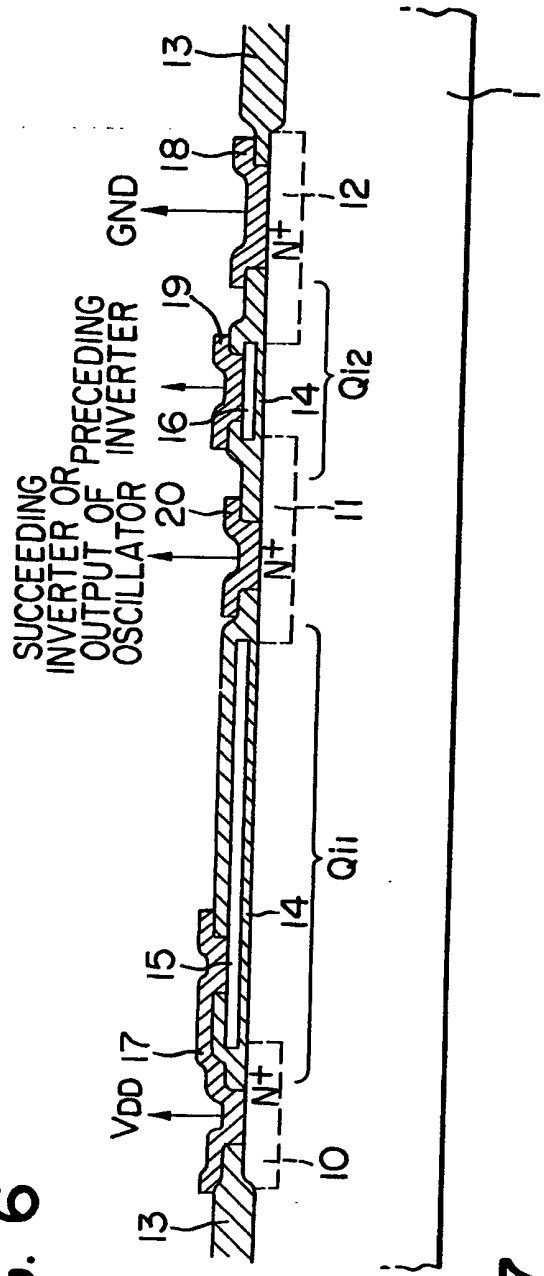


FIG. 6

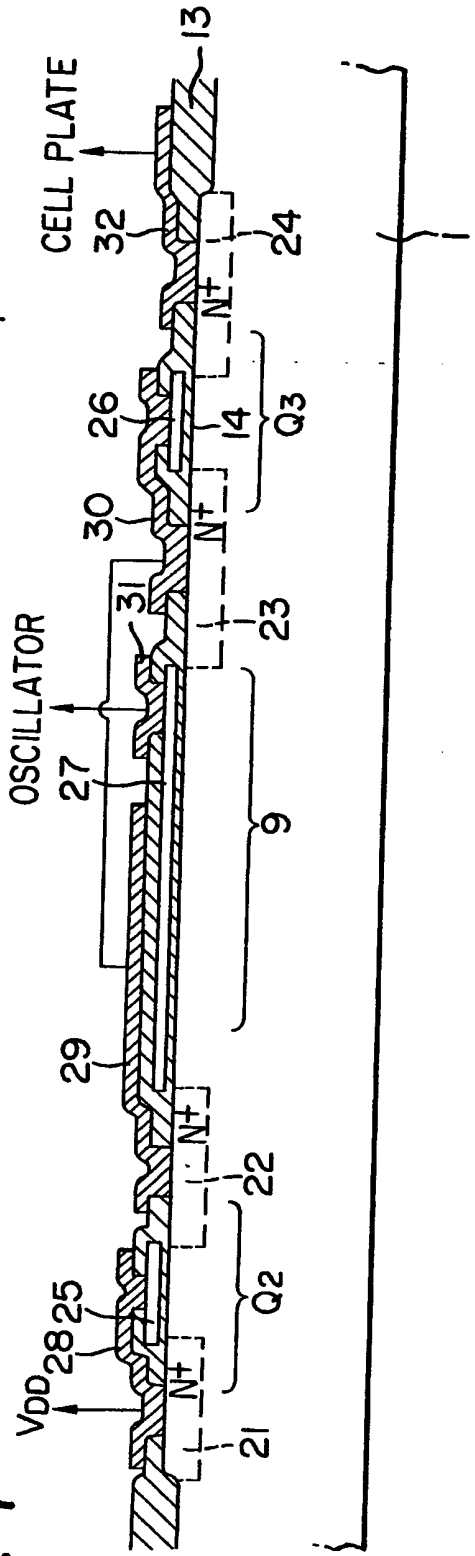


FIG. 7

FIG. 8

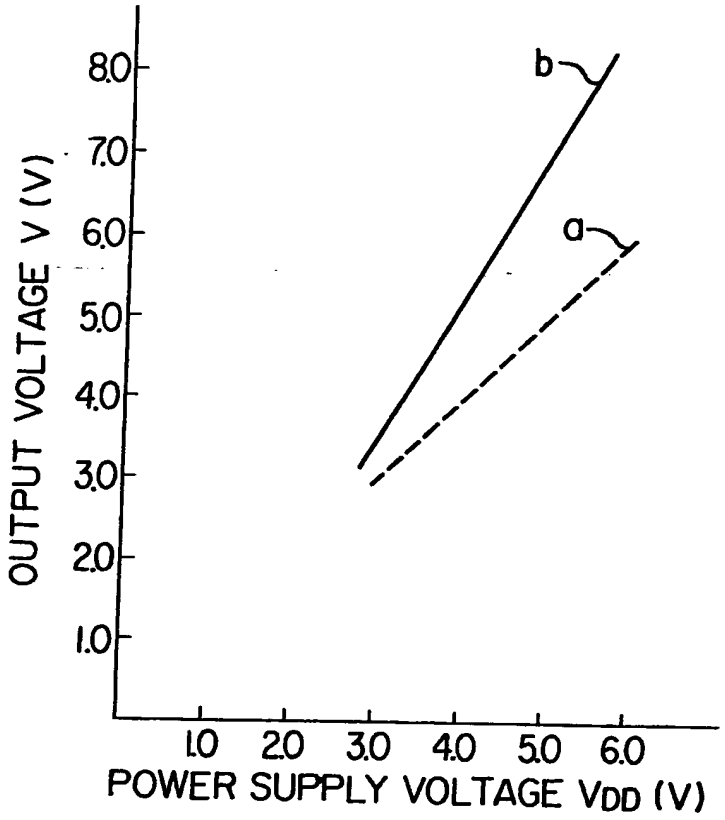
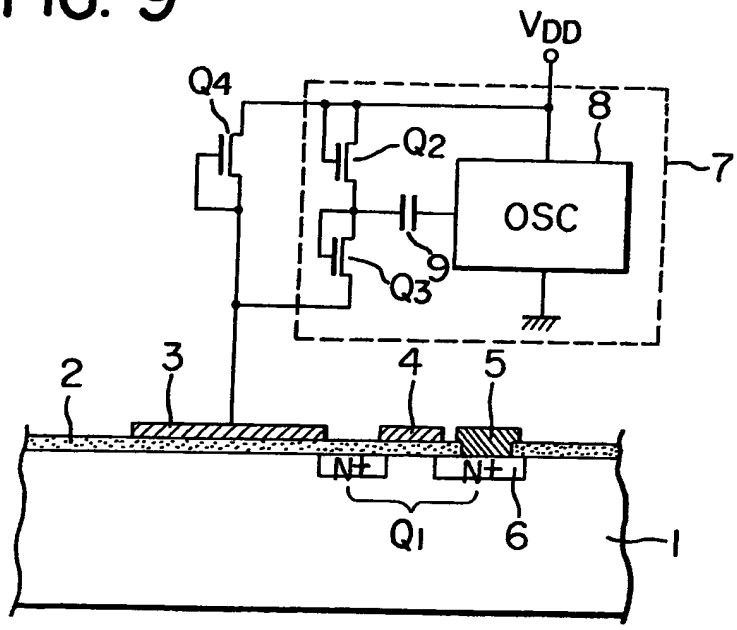

8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
OUTPUT VOLTAGE V (V)
b
a
1.0 2.0 3.0 4.0 5.0 6.0
POWER SUPPLY VOLTAGE VDD (V)

FIG. 9


VDD
Q4
Q2
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OSC
9
Q3
2
3
4
5
N+
N+
Q1
6
1

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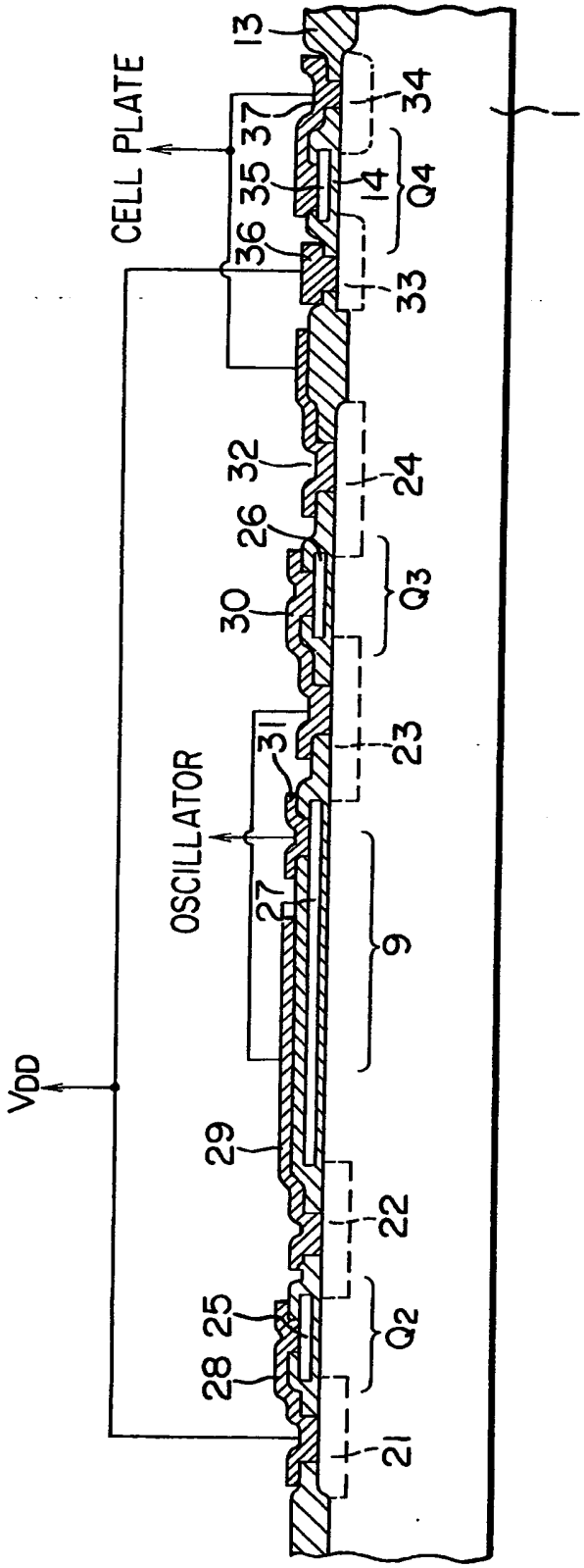
FIG. 10



art semiconductor memory devices so that it is not needed at all to devise a sense amplifier having a higher degree of sensitivity than the conventional one.

As described previously, as compared with the prior art, the present invention can increase the signal voltage by about 70%. It follows, therefore, that when the desired signal voltage may be equal to the signal voltage derived by the prior art, the electric charge stored on the MIS capacitor can be decreased and consequently the capacitor surface area can be decreased accordingly. More specifically the surface area of the capacitor can be decreased by about 40% as compared with the prior art. Thus the present invention provides semiconductor memory devices in an extremely higher degree of packaging density. Even when the cell plate voltage generating circuit is taken into consideration, the semiconductor memory device can be reduced in size by more than 10% as compared with the prior art memory device.

So far the present invention has been described in conjunction with MOS FET, but it is to be understood that the present invention may be equally applied with other types of MIS transistors. The oscillator circuit 8 of the cell plate voltage generating circuit has been described as consisting of the ring oscillator, but it is understood that any other conventional oscillator such as the RC oscillator may be used.

The cell plate voltage generating circuit in both the first and second embodiments has been described as consisting of a unit comprising one oscillator circuit, one capacitor and two series-connected transistors, but it is to be understood that a plurality of such units may be connected in parallel so as to provide a cell plate voltage generating circuit.

In the second embodiment, the voltage limitter circuit has been described as comprising one MIS FET, but it is to be understood that a PN junction with an equivalent threshold value may be used.

CLAIMS

1. A semiconductor memory device of the type comprising:

a semiconductor substrate,

an insulating film formed over said semiconductor substrate, and

a memory cell plate which is formed over said insulating film and functions as a conducting electrode,

whereby a MIS capacitor is provided and the amount of electric charge stored on said MIS capacitor represents a stored information,

characterized by the provision of

a cell plate voltage generating circuit formed on said semiconductor substrate and adapted to generate a DC voltage higher than a power supply voltage supplied to said semiconductor memory device, the output terminal of said cell plate voltage generating circuit being connected to said memory cell plate.

2. A semiconductor memory device as defined in Claim 1 further characterized in that

said cell plate voltage generating circuit comprises an oscillator circuit;

a pumping circuit;

the power supply terminal of said oscillator circuit being connected to a power supply source; and

the output terminal or electrode of said pumping circuit being connected to the output terminal of said cell plate voltage generating circuit while a power supply terminal of electrode being connected to said power supply source.

3. A semiconductor memory device as defined in Claim 2 further characterized in that

said pumping circuit comprises

at least one capacitor;

at least two transistors connected in series;

the output terminal of said oscillator circuit being connected via said capacitor to the junction between said transistors;

the gate of one of said transistors being connected to said power supply source;

the gate of the other transistor being connected to said junction between said two transistors; and

one end of the series circuit of said two transistors being connected to said power supply source while the other end thereof being connected to the output terminal of said cell plate voltage generating circuit.

4. A semiconductor memory device as defined in Claim 2 further characterized in that

said oscillator circuit comprises a ring oscillator.

5. A semiconductor memory device as defined in Claim 2 further characterized in that

said oscillator circuit is an RC oscillator.

6. A semiconductor memory device as defined in Claim 2 further characterized in that

said cell plate voltage generating circuit further comprises:

a voltage limiting circuit.

7. A semiconductor memory device as defined in Claim 6 further characterized in that

said voltage limitter circuit comprises at least one MIS transistor, one end of which is connected to said power supply source and the other end and gate electrode of which are connected to said memory cell plate.

8. A semiconductor memory device as defined in Claim 6 further characterized in that

said voltage limitter circuit comprises a PN junction.

9. A semiconductor memory device, substantially as hereinbefore described, by way of example, with reference to the accompahying drawings.

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